PCI Express® M.2 Specification Revision 4.0 Version 0.3

September 26, 2018

Note to Reviewers:

This specification includes only the high level directions and requirements for the PCI Express 4.0 M.2 specification as approved by the PCIe Mini workgroup. Please provide feedback on these items and any additional requirements that you believe should be covered in the 4.0 M.2 specification.

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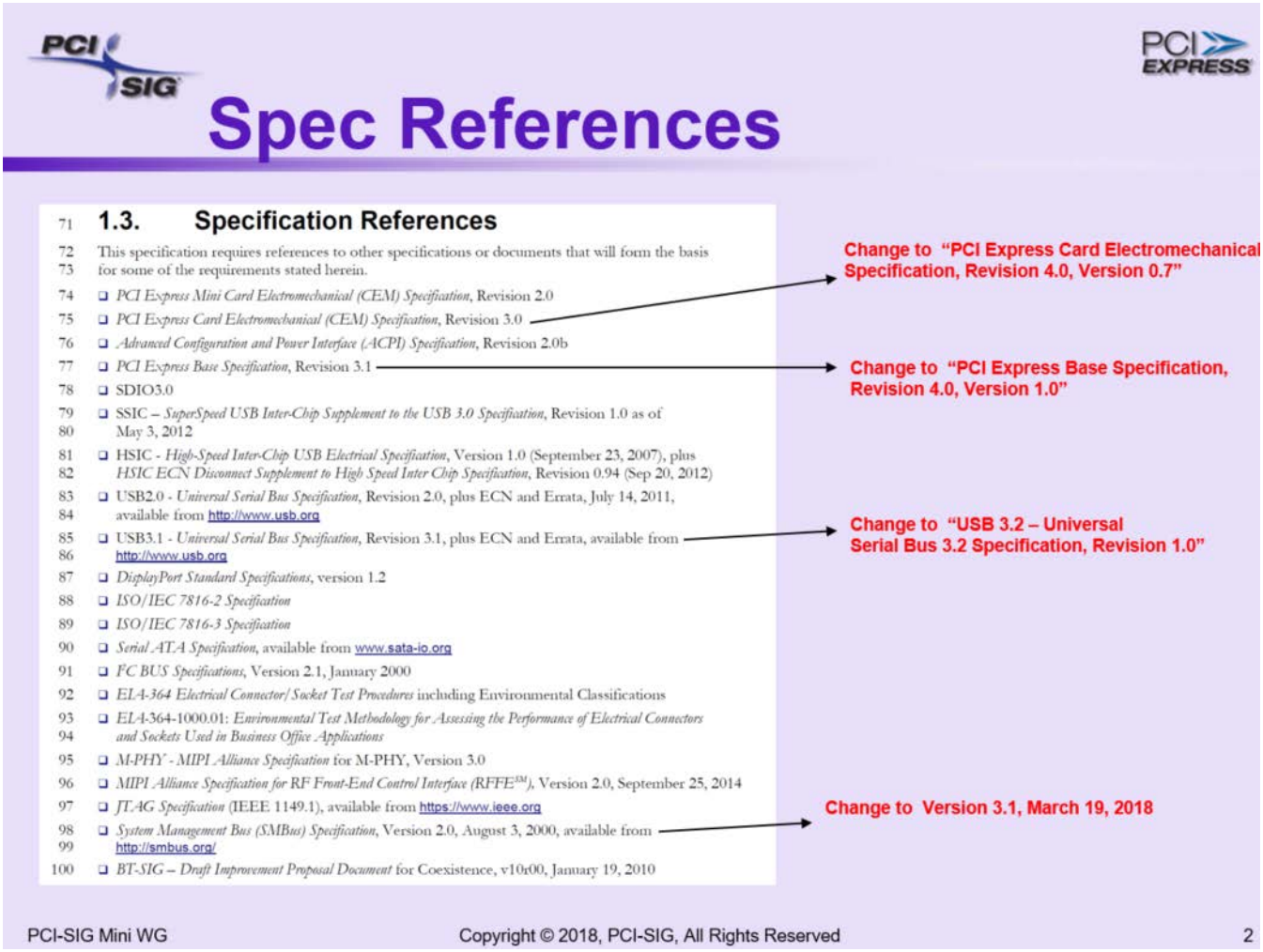
1. **Support signaling rates of 16 GT/s, 8 GT/s, 5 GT/s and 2.5 GT/s**

2. **Specification References list updated to reference the latest specifications:**



3. Clocking

Following clocking architectures will be supported:

a. Common Reference Clock
b. Separate Reference Clock with Independent SSC (SRIS)
c. Separate Reference Clock No SSC (SRNS)

4. No connector changes needed to support 16 GT/s on M.2 connectors. Standalone connector Signal Integrity requirements to be updated as follows:

Signal Integrity Guideline

Table 6-1. Signal Integrity Parameters and Test Procedures for M.2 Connectors

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB up to 4 GHz; ≥ [-0.25*f +0.5 dB for 4 GHz < f < 8 GHz] for example -1.5 dB at 8 GHz ≥ [-0.75*f+4.5 dB for 8 GHz <f<10 GHz For exmple: -3.0 dB at 10 GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≤ -15 dB up to 3.0 GHz; ≤ [5*f - 30 dB for 3.0 < f < 4.4 GHz]. For example: -10 dB at 4 GHz ≤ -8.0 dB from 4.4 to 10 GHz;

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NEXT and FEXT

Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on the M.2 Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max
Differential Near End Crosstalk (DDNEXT) and Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: • The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. • This is a differential crosstalk between a victim differential signal pair and all adjacent differential signal pairs. The measured differential S-parameter shall be referenced to 85 Ω differential impedance.	≤ -32 dB up to 8 GHz and -20 dB from 8 GHz to 10 GHz;

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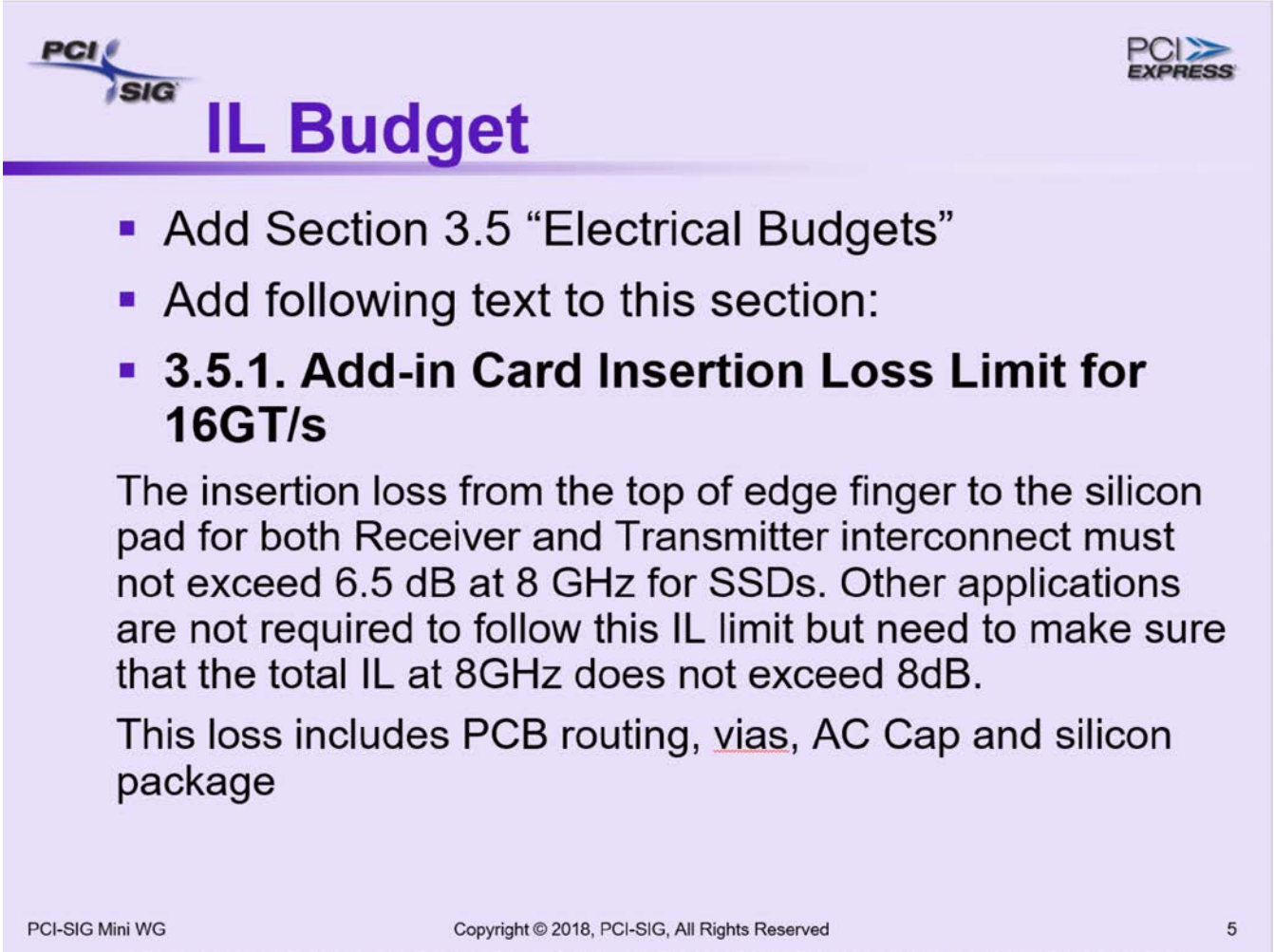
5. Add following IL budget requirements:



6. Add Standalone Connector test guidelines in the Signal Integrity section.

a. Elaborate on the Victim/Aggressor high speed signal pair arrangement to capture worse case cross-talk on the connector.

7. Update the test fixtures recommendations and golden finger Ground voiding guidelines to support 16 GT/s

8. Add Transmitter Equalization details

a. Add Preset test requirements at 16 GT/s

9. Define Eye Diagrams at the Add-in Card Interface

a. Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
b. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s
c. System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
d. System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

10. Define Adapter Transmitter Path Pulse Width Jitter (PWJ) limits at 16 GT/s

11. Define 16 GT/s Test channels and distribute with the specification.

a. System board test channel (S-parameters)
b. Add-in Card test channel (S-parameters)